Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-105 (canceled)

106. (currently amended) A semiconductor chip connected to a wirebond interconnect, ~~or wafer~~ comprising:

a silicon substrate;

a transistor in or on said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate, wherein said first contact pad has a top surface with a first region and a second region, wherein said second region surrounds said first region;

a passivation layer over said metallization structure, over said dielectric layer and on said second region, wherein ~~an~~ a first opening in said passivation layer is over said first region and exposes said ~~a~~ first region, ~~contact pad of said metallization structure,~~ and

wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer; ~~an inorganic material;~~

a polymer layer on ~~over~~ said passivation layer, wherein a second opening in said polymer layer is over said first region and exposes said first region, and wherein said polymer layer has a thickness ~~of~~ between 2 and 50 μm and greater than that of said passivation layer; and

a second contact pad connected to said wirebond interconnect, ~~a metal trace over part of said polymer layer and over said first contact pad,~~ wherein said second contact pad ~~metal trace~~ comprises ~~a~~ an electroplated gold layer with a thickness ~~of~~ between 2 and 100 μm, ~~and wherein said metal trace comprises a second contact pad~~ wherein said second contact pad is connected to said first contact pad through said first and second openings, and wherein the positions of said first and second contact pads from a top perspective view are different.

Claims 107-109 (canceled)

110. (currently amended) The semiconductor chip ~~or wafer~~ of claim 106, wherein said second contact pad ~~metal trace~~ further comprises a titanium-containing layer under said electroplated gold layer.

Claim 111 (canceled)

112. (currently amended) The semiconductor chip ~~or wafer~~ of claim 110, ~~106,~~ wherein said titanium-containing layer comprises tungsten. ~~second contact pad is used to be wirebonded thereto~~.

113. (currently amended) The semiconductor chip ~~or wafer~~ of claim 110, ~~106~~ wherein said titanium-containing layer comprises nitrogen. ~~further comprising a wirebond over said second contact pad.~~

114. (currently amended) The semiconductor chip ~~or wafer~~ of claim 106, wherein said polymer layer comprises polyimide. ~~further comprising a metal bump over said second contact pad.~~

Claims 115-119 (canceled)

120. (currently amended) A semiconductor chip ~~or wafer~~ connected to a wirebond interconnect, comprising:

a silicon substrate;

a transistor in or on said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate;

a passivation layer over said metallization structure and over said dielectric layer,

~~wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and~~ wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer; ~~an inorganic material;~~

a polymer layer on said passivation layer, wherein an opening in said polymer layer is over said first contact pad and exposes said first contact pad, and wherein said polymer layer has a thickness between 2 and 50 μm and greater than that of said passivation layer; and

a second contact pad connected to said wirebond interconnect, ~~first contact pad,~~ wherein said second contact pad comprises ~~a~~ an electroplated gold layer with a thickness ~~of~~ between 2 and 100 ~~15~~ μm, wherein said second contact pad is connected to said first contact pad through said opening, and wherein the positions of said first and second contact pads from a top perspective view are different. ~~; and~~

~~a circuit interconnect wirebonded to said second contact pad.~~

Claims 121-135 (canceled)

136. (currently amended) A semiconductor chip connected to a wirebond interconnect, ~~circuit component~~ comprising:

a silicon ~~semiconductor~~ substrate;

a transistor in or on said silicon substrate;

a metallization structure over said semiconductor substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate, wherein said first contact pad has a top surface with a first region and a second region, wherein said second region surrounds said first region;

a passivation layer over said metallization structure, over said dielectric layer and on said second region, wherein a first opening in said passivation layer is over said first region and exposes said first region, and wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer; ~~an inorganic material;~~

a polymer layer on said passivation layer, wherein a second opening in said polymer layer is over said first region and exposes said first region, and wherein said polymer layer has a thickness between 2 and 50 μm and greater than that of said passivation layer; and

a second contact pad connected to said wirebond interconnect, ~~a metal trace over said passivation layer,~~ wherein said second contact pad ~~metal trace~~ comprises a titanium-containing layer with a thickness between 0.01 and 3 μm, a seed layer with a thickness between 0.05 and 3 μm over said titanium-containing layer, ~~, a first gold layer on said titanium-containing layer,~~ and ~~a second~~ an electroplated gold layer with a thickness between 2 and 100 μm on said seed layer, ~~on said first gold layer, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm, said first gold layer has a thickness of between 0.05 and 3 μm, and said second gold layer has a thickness of between 2 and 100 μm;~~ ~~and~~ wherein said second contact pad is connected to said first contact pad through said first and second openings, and wherein the positions of said first and second contact pads from a top perspective view are different.

~~a circuit interconnect wirebonded to said metal trace.~~

Claims 137-140 (canceled)

141. (currently amended) The semiconductor chip ~~or wafer~~ of claim 110, wherein said titanium-containing layer has a thickness ~~of~~ between 0.01 and 3 μm.

142. (currently amended) The semiconductor chip ~~or wafer~~ of claim 110, wherein said second contact pad ~~metal trace~~ further comprises a ~~another gold~~ seed layer between said titanium-containing layer and said electroplated gold layer, wherein said ~~another gold~~ seed layer has a thickness ~~of~~ between 0.05 and 3 μm.

143. (currently amended) The semiconductor chip ~~or wafer~~ of claim 120, wherein said second contact pad further comprises a titanium-containing layer under said electroplated gold layer.

144. (currently amended) The semiconductor chip ~~or wafer~~ of claim 143, wherein said titanium-containing layer has a thickness ~~of~~ between 0.01 and 3 μm.

145. (currently amended) The semiconductor chip ~~or wafer~~ of claim 143, wherein said second contact pad ~~metal trace~~ further comprises ~~another gold~~ a seed layer between said titanium-containing layer and said electroplated gold layer, wherein said seed ~~another gold~~ layer has a thickness ~~of~~ between 0.05 and 3 μm.

Claims 146-152 (canceled)

153. (currently amended) The semiconductor chip ~~circuit component~~ of claim 136, ~~139,~~ wherein said polymer layer comprises polyimide.

Claim 154 (canceled)

155. (currently amended) The semiconductor chip ~~or wafer~~ of claim 120, ~~123,~~ wherein said polymer layer comprises polyimide.